Impact of Structure, Threshold Voltage, and Noise over the Performance of Pentacene Based OFET: A Comparative Study

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Abstract: *Pentacene based organic field-effect transistors (OFETs) shows an adjustment in threshold voltage which is because of chemical processing in the organic polymer gate dielectric layer that is oxygen plasma treatment to explain this we demonstrate the comparison between OFET device1 untreated called control transistor and device2 determined by O_2 plasma treatment in parylene surface. Pentacene organic field-effect transistor (OFET) consists of the top contact and bottom contact transistor. The top contact structure has high mobility and low contact resistance compared with the bottom contact structure. The organic semiconductor material is assessed with functional parameters like mobility, which tells how fast the electrons or hole moves within the semiconducting layer. The organic transistor has a critical role to play in the application of organic electronic devices, which are used in our day-to-day life. The application of OFET involves the merging of printed electronic and organic transistors, which lead to low cost, mass, and large-scale producers. Variation of noise magnitude, which depends on drain current, is because of photocurrent excitation and the carrier trapped in the boundary of dielectric and semiconductor, which is due to UV-ozone treatment.*

Keywords: *Organic material, transistor structure, threshold voltage, flicker noise.*

1. Introduction

Organic electronics is a branch where we learn how to deal with electronics compactly and flexibly. If we see the past electronics, their size is so big and occupy lots of space, so many heating problems, and the cost is also high. So there are lots of challenges faced by researchers, scientists, and chemists to overcome this problem. These people bring out something which is low cost, compatible, flexible, and used in enormous area implementation such as plastic electronics, electronic textiles, robotic skin [1-5], and biomedical [6]. All these implementations are only possible with the help of a transistor called an organic field-effect transistor. In recent times, pentacene-based organic field-effect transistors demonstrate in "functional logic circuitry and active-matrix liquid crystal display" [7,8]. An organic transistor is manufactured at a low temperature so they are deposited over an extensive flexible substrate, which helps large-area electronics appliances such as billboard displays, i.e., hoardings.

Earlier electronics use organic material in dielectric or packing when we compare organic material with an inorganic material such as silicon, so they are minor in terms of characteristics such as mobility, a threshold, etc. Due to good organic material conductivity and flexibility, it is copying all the devices of conventional or inorganic materials like OLED, OTFT, OFET, and many more. We use organic material in the electronic field because it can propose such a thing which helps us to design a new concept in electronic devices. The organic material consists of lightweight and strong-bearing carbon. Due to weak molecular interaction crystal of organic material is more flexible than silicon. Organic material fabricates devices on the flexible and inexpensive plastic substrate because they consist of the weak molecular structure of OFET. Because of this, it is processed at low temperatures. By using soluble organic material which does not require a vacuum process due to it, printing or coating technology comes into the picture to construct appliances for the wide surface area along with fewer prices.

We have evaluated the electrical characteristics of different structures, i.e., bottom contact, and top contact structure pentacene. Here thermal evaporation process is applied for the deposition of pentacene semiconductors [9]. The structures we have demonstrated have mobility $0.2 cm^2/Vs$ and $0.02 cm^2/Vs$. The effectiveness of organic semiconductors is usually measured by mobility, which is improved by research on the material over the last few decades. The report published by D. Gamota et al. [11] depicts how with limited assumptions, we can extract the field-effect mobility directly. And also, take a review on the threshold voltage which states circuit usefulness and output means that how the threshold voltage and conductivity adjusted according to the gate dielectric i.e., O_2 plasma treatment of the gate dielectric, which increases drain current in OFET characteristics [12]. Due to O_2 treatment bond breaks in parylene surface, which produces interface states in which charge generates which help in a shift of threshold voltage and bulk conductivity. The working of OFET in accumulation mode is accompanied by the method of trap governed by the hopping process [13]. The power level of flicker noise ($\sim 1/f^{ß}$, $ß \approx 1 \pm 10\%$) is more in OFET than conventional semiconductor-based MOSFET due to the high amount of scattering place within molecules and traps [14]. Here we determine on comparing noise characteristics of OFET devices for evaluation of noise, which contributes to boundary states that are one OFET device where gate dielectric treated with UV-ozone before the semiconductor layer and another device is free from oxygen and water vapor atmosphere.

2. Discussion

Pentacene is the polyaromatic hydrocarbon which contains ∏ bond which is formed by overlapping of p-orbital's which are present in aromatic rings contain alternating single and double bonds are called conjugated organic molecules, which result in the delocalization of ∏ electron, and it is available in the market widely as well as exhibits high hole mobilities for a polycrystalline film. A report by Lin et al. [15] depicts mobility of $1.5 cm^2/Vs$, On/Off current ratio$>10^8$, near-zero threshold voltage, and a subthreshold slope$<$ 1.6 V/decade. To show high performance, it is fabricated with a polymer dielectric, which has high carrier mobility up to $3cm^2/Vs$. The subthreshold fluctuation is minimized to 1.2 V per decade, and the On/Off current ratio $\sim 10^5$. High-performance pentacene is prepared from the flow of hydrogen or nitrogen in the vapor phase [16], and it is fairly steady to oxygen, light, and ambient condition [17]. The charge transport and OFET performances are control by semiconductor film morphology and microstructure [18], chemical structural, quality of the semiconductor/dielectric interface, the surface roughness of the gate dielectric [19]. Mobility and On/Off current ratio, variation is seen in pentacene when analysis of OFET dielectric-semiconductor interfacial is performed with different high-k metal oxides as gate dielectric such as SiO_2, Al_2O_3, TiO_2, etc. [20].

2.1 OFET Structures

There are two types of pentacene OFET structure, as these structures impact the electrical characteristics of pentacene OFET such as a) Top contact b) Bottom contact. Both structures working in accumulation mode and that hole is the majority charge carrier because of the p-type semiconductor that is pentacene see in figure 1 [21].

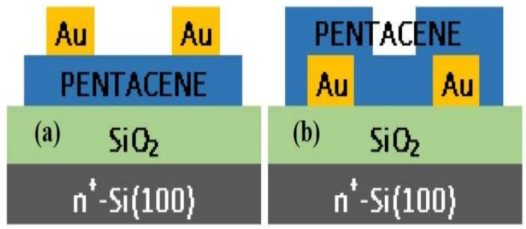


Figure 1. a) Top contact transistor b) Bottom contact transistor based on pentacene as a semiconducting layer.[21]

The top contact transistor has a high mobility of the hole as a comparison to the bottom contact due to which high current is produced. Bottom contact has low mobility due to grain boundaries which trap the charge. In both cases, differences in current are more than the differences in mobility. In top contact transistors, it is difficult to fabricate small channel lengths whereas bottom contact transistors not. Here mobility and drain current is measured by [21]:

$$\mu = \frac{2L\left[\frac{\partial\sqrt{I_d}}{\partial V_g}\right]^2}{WC_i} \qquad (1)$$

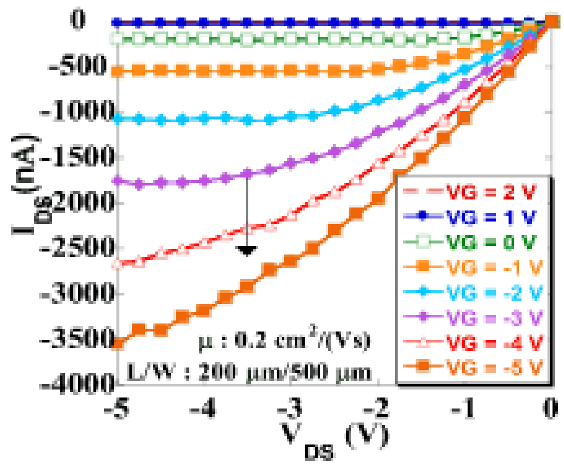
$$I_d = \frac{W\mu C_i}{2L}\left(V_g - V_T\right)^2 \qquad (2)$$

Where, V_T- Threshold voltage, L- Channel length, μ- Mobility, W– Channel width, I_d- Drain current, V_g - gate voltage, C_i- Gate insulator capacitance per unit area.

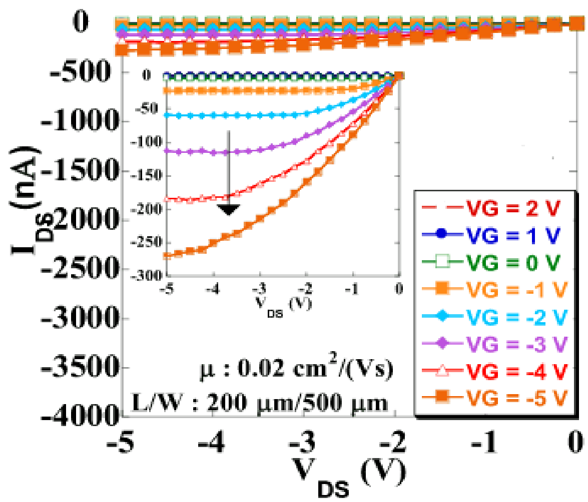
Figure 2 [21] exhibits the I-V characteristics which correlate with the structure. Its shows that the top contact pentacene structure exhibit superior mobility and drain current than that of bottom contact. In table 1 these two parameters are compared when these are calculated for the given data L/W: 200 / 500 at V_{GS}=V_{DS}= -5V. Where V_{GS} is a gate to source voltage and V_{DS} is a drain to sources voltage

Table 1. Comparison between Top and Bottom Contact

Terms	Top Contact	Bottom contact
Mobility (cm^2/Vs)	0.2	0.02
Drain current(nA)	3500	275



(a)



(b)

Figure2. I_D-V_D characteristics of different structures of pentacene OFET (a) Top Contact (b) Bottom Contact [21].

From the above table 1, we come to know how the top contact structure is much better than the bottom contact. Bottom contact structures have their existence in humidity sensors as the decrease in hole mobility due to interaction of water molecules in grain boundaries [22]. We can enlarge the mobility of the bottom contact transistor by introducing a buffer layer like PMMA at the interface of the gate insulator and organic semiconductor, which provide free electrons and reduce contact resistance [23].

We can determine the ac characteristics with the help of the Capacitance-Voltage curve which tells about the frequency at which organic semiconductor performs better [24], according to the research accumulation region is seen at a low frequency so that for high-frequency appliances organic semiconductor are not appropriate as it has less mobility and not provide an immediate response to AC signal [25]. Because of the advancement in an organic semiconductor, it can be implemented in the digital logic circuit for instance NAND gate, inverter, NOR gate, and SR latch all work at various kHz.

2.2 Threshold voltage

Differences in threshold voltage are generally because of the presence of a fixed charge state that is process-dependent at the boundary of semiconductor and dielectric. In table 2 OFET, based on hole-conducting pentacene generates the range of threshold voltage

Table 2. A different process for different voltage

Threshold voltage	Process	Polymer dielectric material	Ref.
Positive voltage	Solution-processed	PVP	[2]
Negative voltage	Chemical vapor decomposition (CVD)	Parylene	[26]

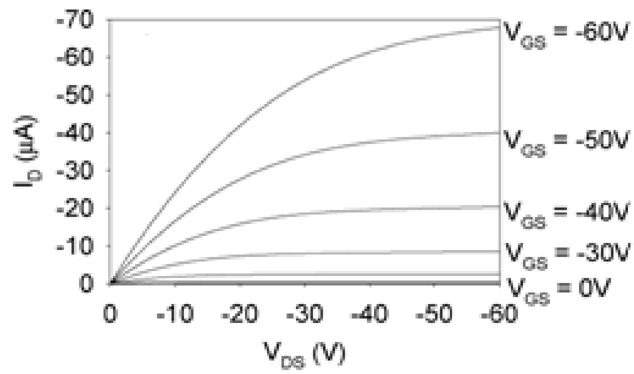
The CVD polymer parylene is fully cross-linking during deposition which solution-processed not. We show about pentacene OFET with parylene gate dielectric in which dielectric is treated with O_2 plasma before pentacene deposition which forms a parylene-pentacene interface state and these state dope the semiconductor and produces two types of charges such as mobile charges which enhances parasitic bulk conductivity in the devices and fixed charges which variates the threshold voltage and increase the drain current.

The experiment is performed to describe the above point we are taking two sets of devices to see In table 3 that are fabricated on a glass substrate with the gate dielectric using parylene-C with the top contact structure with a 275±5 nm of parylene layer like a blanket was deposited using CVD process over the structured gate, 10 nm of pentacene layer with the help of thermal evaporation lie on parylene after then electron beam deposition is used for source and drain contacts with channel length and width are 42μm and 1250 μm[12]. Where device 1(Untreated) fabrication consist of gates use aluminum, semiconductor uses pentacene layer, and source/drain contacts use gold formed with the help of a shadow mask, and parylene-C is used as a gate a dielectric use CVD process for the deposition over structured gates and in device 2(treated), equivalent substances are required for gates, the semiconductor layer, gate dielectric, which device 1 required alongside the O_2 plasma on the parylene surface before 15 seconds of pentacene deposition and it has top contact OFET device structure and we founded on comparing both results in device 2 give a better result in terms of current, conductivity, and threshold voltage.

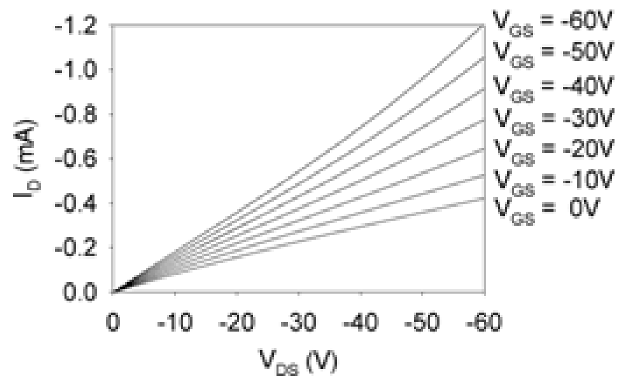
Table 3. Comparison of Devices before and after treatment

Terms	Device 1 (untreated)	Device 2 (treated)

Drain current (I_D)	The current is low, saturate see figure 3(a) [12].	The current is high but does not saturate see figure 3(b) [12].
Conductivity	Not have high significant parasitic bulk Conductivity	High significant parasitic Bulk conductivity
Threshold Voltage (V_T)	By evaluation of saturation region, we can withdraw V_T.	Here V_T withdraws from the V_{GS}, which is near to V_T but not from the saturation region.



(a)



(b)

Figure 3. I-V Characteristics of OFET Devices (a) Device 1 (untreated), (b) Device 2(treated) [12].

In figure 4 we can exhibits how the threshold voltage variation takes place due to oxide treatment in pentance based OFET and due to the increase in current the threshold voltage tends toward positive voltage that is from -17V to 116V then the relative threshold voltage which we get that is +133V help in calculating fixed charge in devices 1 and 2.

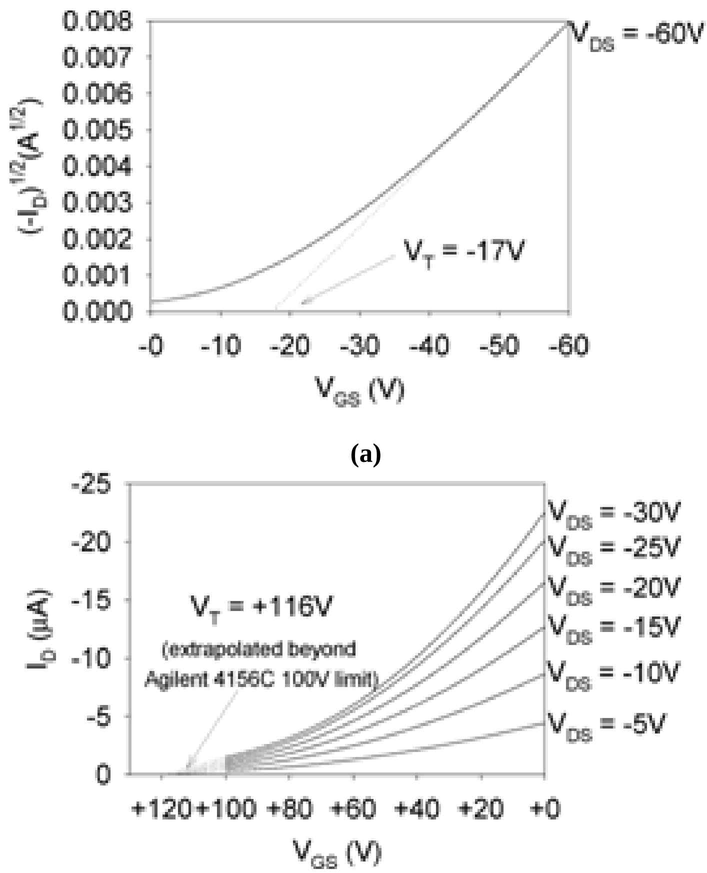


Figure 4. Threshold Voltage of OFET Devices (a) Devices 1 (b) Devices 2 [12].

Enhancement of current in device2 is not due to the chances of modification in pentacene structure such as mobility of field-effect is responsive to the grain size of pentacene [10], increase in field-effect mobility, this is basically because of threshold voltage and bulk conductance which shows the increment of I_D in the linear region of OFET operation. In OFET interface states which consist of mobile and fixed charge contribute to the linear region, and more often, these are modeled with the help of devices equations used in conventional semiconductors see equation 3 [27]. The model consists of 1) Carrier density present in the surface channel due to the accumulation layer is modified by the gate voltage, and 2) the gate voltage is not modulated from the mobile carrier density, which is in the bulk layer, which is away from the surface channel. So adjustment in threshold voltage is because of a fixed charge, and parasitic bulk conductivity is due to the mobile charge.

$$-I_D = \frac{W}{L}\mu V_{DS}\left[C_{ins}\left(V_{GS} - V_T - \frac{Q_{fixed}}{C_{ins}}\right)\right] + \frac{W}{L}\mu V_{DS} Q_{mobile} \qquad (3)$$

Where, W=Width, L=Length, C_{ins}= Capacitance of dielectric insulator, μ =Mobility of field effect, V_T= Threshold voltage, V_{GS}= Gate-Source voltage, V_{DS}= Drain-Source voltage, Q_{fixed}= Fixed boundary charge, Q_{moblie}= Parasitic mobile charge. Q_{fixed} and Q_{moblie} are obtained from I-V characteristics. The O_2 plasma treatment devices introduce traps in the interface, which are observed by capacitance measurement of MIS test structures and photocurrent measurements of

OFET [12]. When we are discussing transistors so capacitance measurement through the C-V curve comes into the picture here also the same but little bit of change in the C-V curve because of oxygen plasma treatment. In device 2 C-V curve exhibit accumulation mode overall instead of the flat band and depletion mode, which device 1 can exhibit in the range -45 to 45; this is due to treatment see in figure 5 [12].

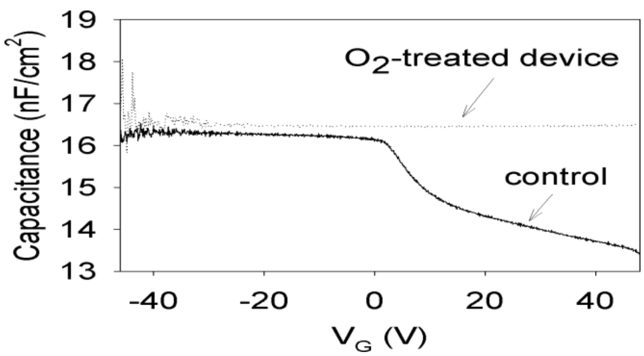
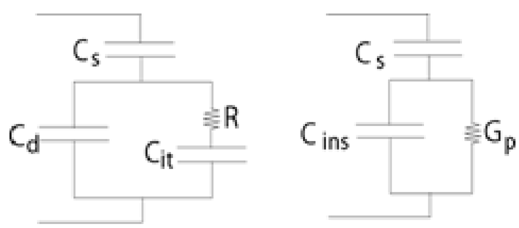


Figure 5. C-V curve of device 1 shows all accumulation, flat band, and depletion mode which device2 does not, only accumulation region [12].

To understand the trap, which is the cause for threshold voltage adjustment, we stimulate traps as capacitances for RC time constant correlate with trapping as well as exposure of carriers[28],[29]. So we stimulate the boundary of the semiconducting layer and gate dielectric with three capacitors they are C_s, C_d, and, C_{it} as shown in figure 6(a) [12]. C_{total} is the overall capacitance.

$$C_{total} = \left(\frac{1}{C_s} + \frac{1}{C_d + C_{it}}\right)^{-1} \qquad (4)$$

Where C_s indicate capacitor formed from semiconductor depletion, C_d capacitor formed from a dielectric (parylene) and, C_{it} capacitor formed from the trap and these traps in the form of parasitic RC leg is stimulated parallel with dielectric. In the accumulation mode peer model of the capacitor is seen where C_{ins} is a parallel connection of C_d and C_{it} see in figure 6(b) [12].



(a) (b)

Figure 6. (a) Interface model of the capacitor (b) Model of the capacitor at accumulation mode [12].

As discussed above, the adjustment in threshold voltage is determined by the growth of boundary trap concentration in device 2. So to measure the trap which is produced by O_2 exposer is also evaluate by photocurrent where de-trapping of the carrier is produced by photons which stuffing the boundary trap and discharge extra charges which support for conduction.

2.3 Flicker Noise

As discussed when we expose dielectric to oxygen plasma treatment that leads to the adjustment of threshold voltage, same here in the case of noise evaluation which depends on drain current

when we expose the parylene dielectric to UV- ozone treatment which results in the interface traps were hopping of the carrier take place when compared with control transistor with no treatment leads to the evaluation of *1/f* noise on pentacene OFET, to understand the discussion we will perform the experiment which consists of two sets of device they are device 3(untreated) called as control OFET and device 4(treated). These devices use a glass substrate for the fabrication; shadow masking is used for patterning source-drain contact, the semiconductor layer, and the gate. The structure of devices 3 and 4 composed of 60 nm thick gate electrode made of Al using thermal evaporation accompanied by 200 nm gate dielectric (parylene-C) processed by chemical vapor deposition (CVD), vacuum evaporation used for layering 25nm of pentacene on a substrate at a rate of 0.1-0.2 A/s, Au source-drain contact uses thermally evaporation. All mentioned earlier take place in the glovebox cluster; it has less than 0.1 ppm for oxygen and water vapor, which are wiped constantly. Meanwhile, the device 4 gate dielectric is subjected to air and 20 minutes before the pentacene deposition dielectric is processed by air-generated mercury lamp UV-ozone [12], were as device 3 is processed in the absences of oxygen and water vapor, both devices have the same channel length and width (L/W= 50μm / 860μm) [30].
In figure 7 [30] reveal the exciting voltage of device 4, which is adjusted to the positive voltage because of the negative charge trapped in the boundary of semiconductor and dielectric [12], [31]. This adjustment of voltage is due to ozone treatment [33]. UV ozone treatment at the surface of the dielectric leads to the electron-accepting place of –COOH and OH groups [33], [34], which help in generating holes from pentacene because the electron is removed [35], [31]. The fixed negative charge developed from trapped electrons leads to accumulating holes, increases the noise level, and acts as scattering sites.

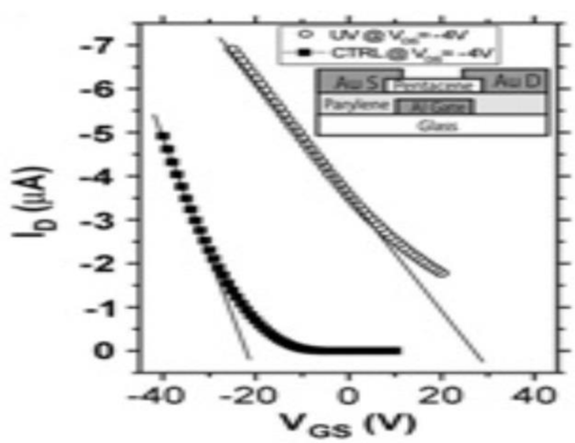


Figure 7. Threshold voltage tuned to positive voltage due to UV ozone treatment in a transistor (shown in a white circle) when compared with a control transistor (shown in a black square) [30].

The flicker noise in OFET is because of the hopping of the carrier among the trap place. Formula express the noise power density in a transistor [36] given as

$$S_f = \frac{K_f}{C_{ox}L^2} \cdot \frac{I_D^{\alpha}}{f_{\beta}} \qquad (5)$$

Where L- Channel length, C_{ox}- Dielectric capacitor per unit area, f- Frequency (Hz), K_f – Coefficient of fractional flicker noise, α, and β are the constants associated with noise-producing states, α ~1-2 and β ~ 1± 10%.

When the gate voltage is switch to the negative side, in that case, devices are in accumulation mode, so noise level increases see in figure 8 [30]. The traps produce in device 4 due to UV lie outwardly to the HUMO-LUMO gap. As noise increase linearly which is because of scattering of the carrier with a constant number due to no change in fermi level seen. With a change in gate voltage as Fermi level cannot access these trap states [31], so α= 1.1 was as in control device that is device 3 response of noise is superlinear with α= 1.6 were change in Fermi level because of gate voltage increase the carrier with scattering states.

To introduce charge into the devices which we discussed above through UV-ozone treatment, now we will discuss with photocurrent excitation. In photocurrent excitation, the fermi level is not altered with the charge produces by it. It allows characterizing the noise in the absence of input voltage.

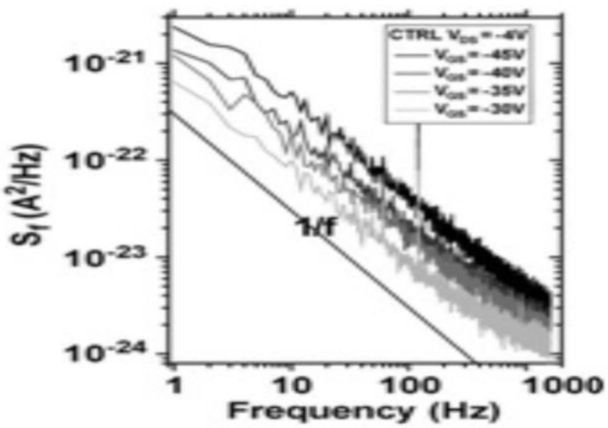


Figure 8. The spectrum of noise power for device 3 [30].

It was demonstrated that the carrier from the boundary of pentacene and gate dielectric is excited with 405nm brightness which is governed by LED, because of brightness photocurrent level increase in device 4 as compared to devices 3 because of the excited carrier we can figure out this in the graph between ΔI_D / I_{D_Dark} = (I_D-I_{D_Dark}) / I_{D_Dark} where I_{D_Dark} – drain current before brightness and I_D – drain current during brightness see in figure 9 [30] it exhibits alteration in drain current when V_{DS} = - 4V, but V_{GS} = - 40V for device 3 and V_{GS} =0V for device4 and the black circle indicates to CTRL, means device 3 while white circle and square indicate UV1, UV2, means device 4 having different α value [30].

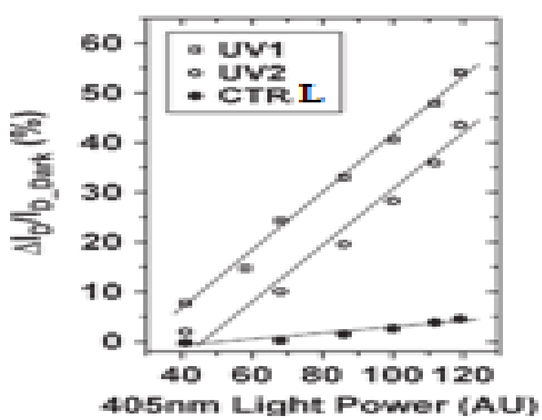


Figure 9. Modification of drain current which is a function of brightness power when subjected to 405 nm LED brightness [30].

There has been noticed that the noise magnitude produced by the gate accumulated is not much high as compared with the carrier produce from the photon because of this slope of noise characteristics increase in device 3.

Conclusion

Pentacene as a semiconducting layer plays a major role in carrier supply, which shows the variation in mobility. Pentacene OFET electrical characteristics vary with the change in the structure, i.e., top contact, and bottom contact. The adjustment is seen in threshold voltage when we do O_2 plasma treatment in the control transistor that is in devices1 because of this treatment interface trap is formed, which is responsible for a fixed and mobile charge, which helps in increasing current so we found on comparison device 2 shows much good result. We reviewed the impact of UV-ozone treatment on the layer of the gate dielectric on the evaluation of 1/f noise in OFET.

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